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REMARKS

The Examiner rejected Claims 1-9 under 35 U.S.C. 102(e) as being anticipated by Zeitler, *et al* (hereafter "Zeitler") (US 2004/0210 693). Applicant submits that Claim 1 and the claims dependent therefrom, as amended above, are not anticipated by Zeitler. Applicant traverses this rejection with respect to Claims 6 and 9.

The Examiner has the burden of showing by reference to the cited art each claim limitation in the reference. Anticipation under 35 U.S.C. 102 requires that each element of the claim in issue be found either expressly or inherently in a single prior art reference. *In re King*, 231 USPQ 136, 138 (Fed. Cir. 1986); *Kalman v. Kimberly-Clark Corp.*, 218 USPQ 781, 789 (Fed. Cir. 1983). The mere fact that a certain thing may result from a given set of circumstances is not sufficient to sustain a rejection for anticipation. *Ex parte Skinner*, 2 USPQ2d 1788, 1789 (BdPatApp&Int 1986). "When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference" (*In re* Rijckaert, 28 USPQ2d, 1955, 1957).

With respect to Claim 4, the Examiner stated that Zeitler also discloses that each of said buses (208a-208e, Fig. 2) is a serial bus. The Examiner does not point to any teaching in Zeitler to that effect. Furthermore, Applicant can find no such teaching in Zeitler. Accordingly, there are additional grounds for allowing Claim 4.

As to Claim 5, the Examiner stated that Zeitler also teaches that the two-dimensional array of nodes comprises a rectangular array in which said network nodes are organized as a plurality of rows and columns. The Examiner has not pointed to any place in Zeitler at which this teaching can be found. Furthermore, Applicant can find no mention of rows and columns in Zeitler. Accordingly, Applicant submits that there are additional grounds for allowing Claim 5.

As to Claim 6, the Examiner asserts that Zeitler teaches first and second substrates satisfying the limitations of Claim 6 with respect to the two-dimensional array of processors and network nodes, which overlie one another. The Examiner points to clusters 101 and 105 in

support of this assertion. The Oxford Concise Dictionary defines a substrate as a surface on which something is deposited or inscribed. The Examiner has not pointed to any teaching in Zeitler that clusters 101 and 105 are on separate substrates, no less that these substrates overlie one another. Accordingly, Applicant submits that the Examiner has failed to satisfy his burden under 35 U.S.C. 102, and hence, the rejection of Claim 6 is improper. The above amendments merely put Claim 6 in independent form.

With respect to Claim 7, the Examiner stated that Zeitler teaches that interconnection controller 230 specifies the connection information that is stored in each of the network nodes. The Examiner points to [0036] as supporting this assertion. Applicant must disagree with the Examiner's reading of the cited passage. The paragraph in question describes the information stored in the routing tables associated with the nodes attached to a controller 230. The paragraph does not state how the information is placed into these tables. Applicant can find no teaching that controller 230 specifies this information for each of the nodes in the system, i.e., each of the nodes in cluster 101. Hence, there are additional grounds for allowing Claim 7.

With reference to Claim 8, the Examiner stated that Zeitler also discloses I/O interfaces 216 and/or 220 provide an interface for receiving the connection information stored in the routing tables from an external source. The I/O interfaces in question connect the components to external devices and networks. However, the Examiner has not pointed to any teaching that the information in the routing tables is provided through one of these interfaces. Hence, there are additional grounds for allowing Claim 8.

With reference to Claim 9, the Examiner maintains that Zeitler teaches that one of the controllers 230 is a spare processing block that is capable of performing processing functions normally performed by a second one of the controllers if the second controller is defective. The Examiner cites the teachings in paragraph [0027] as supporting this assertion. The paragraph in question merely teaches that there are multiple controllers and that the controllers can perform a number of functions. However, there is no teaching that a controller that is attached to a specific set of nodes can replace the functions of another controller that is attached to a different set of nodes. Second, there is no teaching that any of the controllers is a spare controller. Accordingly,

Applicant submits that the Examiner has not met the Examiner's burden with respect to Claim 9. The above amendments to Claim 9 merely place the claim in independent form.

I hereby certify that this paper is being sent by FAX to 571-273-8300.

Respectfully Submitted,

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